REMARKS/ARGUMENTS

Prior to this amendment, claims 2-7, 9-14, and 16-26 were pending. In this amendment, claims 2, 4, 16, 18-20, 22, 24 and 26 are amended. Claims 21, 23, and 25 are canceled without prejudice and without disclaimer. No claims are added. No new matter is added. Thus, after entry of this amendment, claims 2-7, 9-14, 16-20, 22, 24, and 26 will be pending.

Objections to the Drawings

The drawings are objected to under 37 C.F.R. 1.83(a) for not showing every feature of the invention specified in the claims. Regarding claims 22, 24 and 26, it is asserted that the recitation of where the input register has "... an output coupled to an input of the multiplexer" is not shown. This claim element no longer appears in these claims. Accordingly, Applicants respectfully request withdrawal of this objection.

Objection to Claim 24, Informality

Claim 24 is objected to because of an informality. Claim 24 has been amended as suggested by the Examiner. Applicants respectfully request withdrawal of this objection.

Rejections under 35 U.S.C. § 112, written description

Claims 22, 24 and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Office Action asserts that the original specification does not connect "the input register output directly back to an input of the multiplexer." *See* Final Office Action mailed April 11, 2007, page 4 (emphasis added). Applicants still maintain that the word "directly" has been improperly added to these claims.

Nonetheless, the phrase at issue has been removed from these claims. Accordingly, Applicants respectfully request withdrawal of these rejections.

Claim Rejections 35 USC § 112, indefiniteness

Claims 22 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for citing antecedence issues that were already cited in respective preceding claims 21 and 25. Claims 22 and 26 have been amended to be in independent form and to include only one

recitation of the claim elements at issue. Accordingly, Applicants respectfully request withdrawal of these rejections.

Claim Rejections 35 USC § 103(a), Herron, Jin, Suzumura

Claims 22, 24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herron et al., (herein Herron), U.S. Patent No. 6,996,758, and further in view of Jin, U.S. Patent No. 6,114,892 and further in view of Suzumura, US Patent No. 7,058,867.

Claims 2-7, 22

Claim 22 is allowable over these cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 22. For example, claim 22 recites:

> *the input register having an input coupled to an output of a multiplexer and an output coupled to a first input of a logic gate, where a select input for the multiplexer is coupled to a second input of the logic gate and an output of the logic gate is coupled to an input of the IP core, wherein the output of the logic gate provides an output signal to an input of the multiplexer, and wherein the output of the input register provides a signal to an input of another input register in the set of boundary scan registers.*

In Suzumura, the Q˜ output (inverse of Q) of a flip-flop 21A is fed back to the MUX 22a, which provides the D input to the flip-flop 21A. *See Suzumura*, FIG. 1. The purpose of feeding the inverse signal back is to toggle a signal back and forth to accurately test the maximum frequency. *Id.*, col. 3 lines 6-11 and col. 4 lines 47-60.

A combination of Suzumura with the scan flop cell 220 of Jin would then have a feedback signal sent from the NQ' output (corresponding to the Q˜ output of Suzumura) to the DI input of multiplexer 226, and not the Q' output. *See Jin*, FIGS. 3 and 4. Note that it is the Q' output, not the NQ' output, that is sent as the SO output to another scan flop cell. *Id.*, FIGS. 3 and 7.

Thus, the combination provides a feedback signal corresponding to the inverse of SO output and not corresponding to the SO output. Accordingly, the combination of Herron, Jin, and Suzumura does not teach or suggest the same output of a scan register that is coupled to the

logic gate that provides a signal to the multiplexer and that provides a signal to another input register, as recited in claim 22.

For at least the reasons stated above, Applicant submits that claim 22 and its dependent claims are allowable over the cited references.

Claims 9-14,16-20, 23, 26

Applicants submit that independent claims 24 and 26 and their respective dependent claims are allowable for at least the same reasons as claim 22.

Claim Rejections 35 USC § 103(a), Herron, Jin, Kiryu

Claims 4-7, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herron in view of Jin and further in view of Kiryu et al. (herein Kiryu), U.S. Patent Application Publication No. 2005/0138509. The cited teaching of Kiryu fails to make up for the deficiencies of Herron and Jin with respect to the independent claims 22 and 26, from which claims 4-7 and 18 respectively depend. For at least these reasons, claims 4-7 and 18 are allowable of these cited references.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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